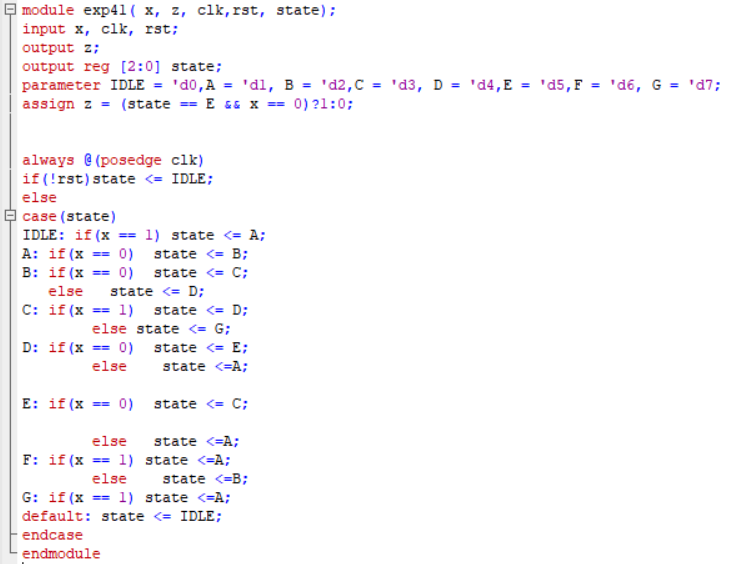
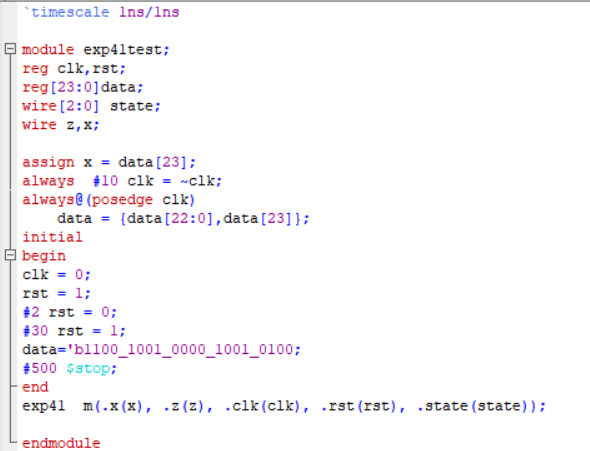
**练习八 利用有限状态机进行时序逻辑设计**

1. **简单状态机设计：**

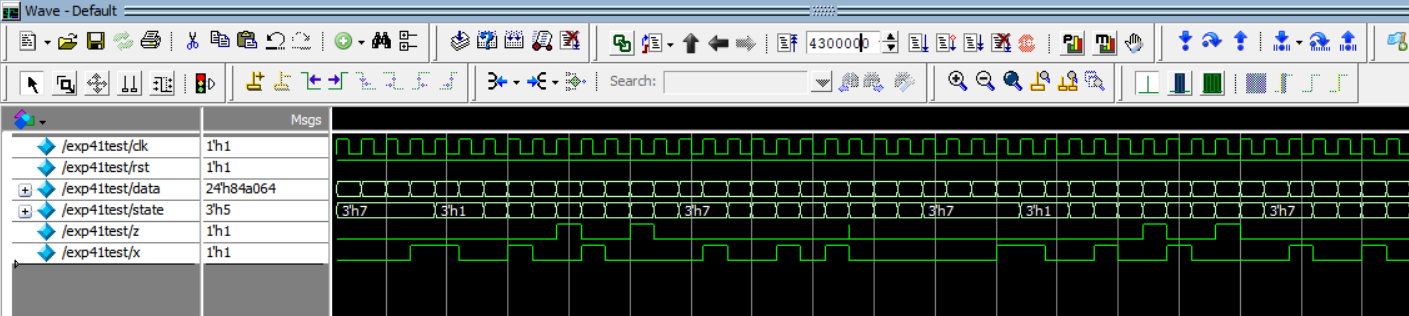
**模块源代码：**

****

**测试模块代码：**

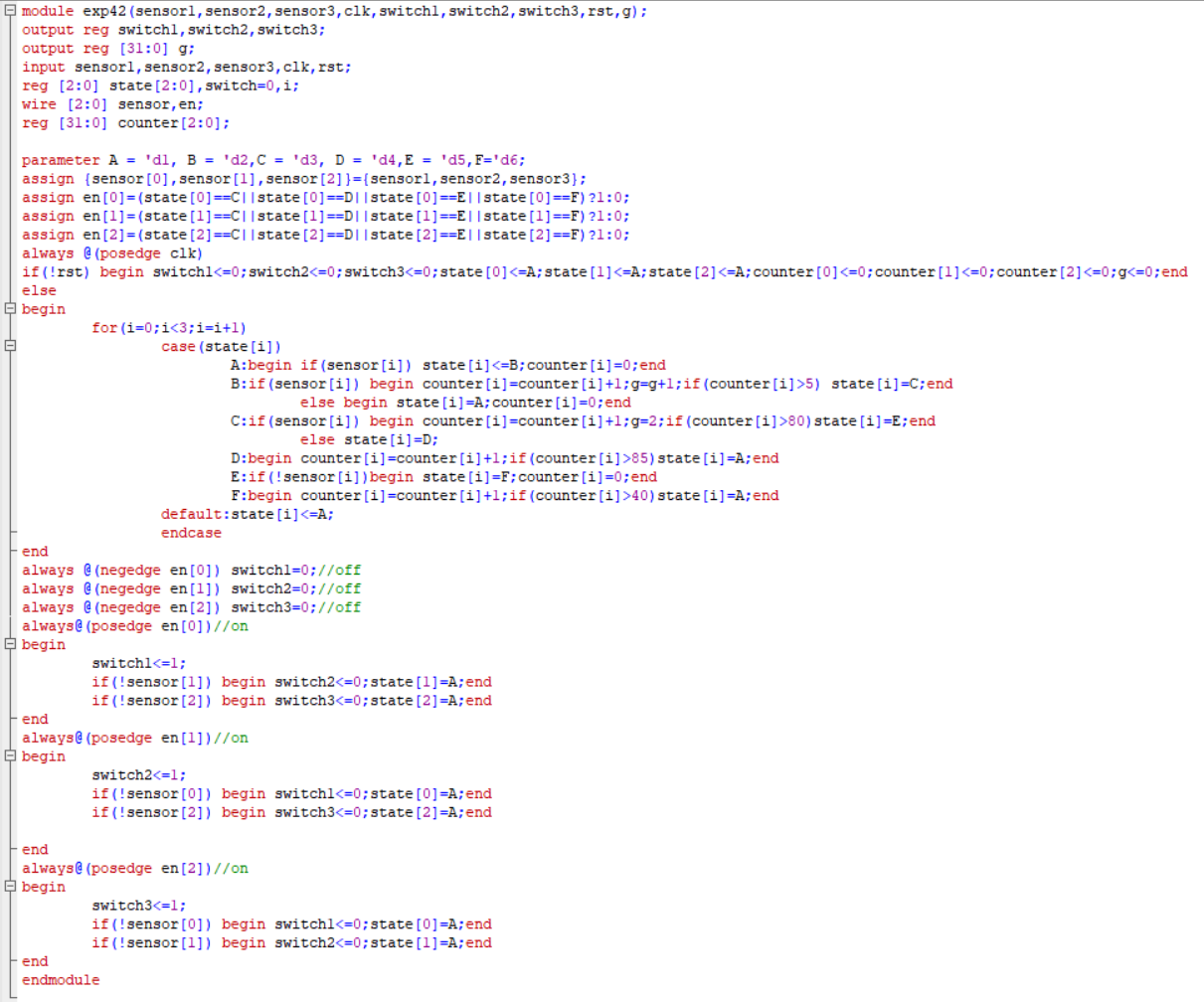
****

**输出结果：**

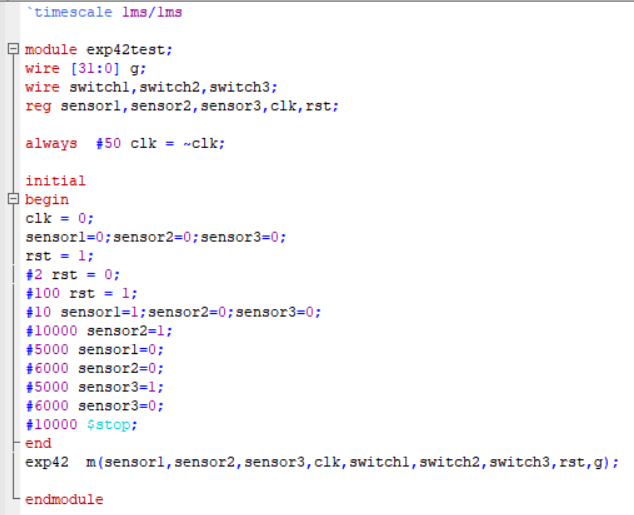


**练习：串行数据检测器：**

**模块源代码：**



**测试模块代码：**



**输出结果：**

